LEAKAGE POWER SAVING TECHNIQUES FOR DEEP SUB-MICROMETER DIGITAL INTEGRATED CIRCUITS

Presented by Vo Minh Huan

Feb 19, 2014
Motivation
- Limited power budget
- ITRS roadmap
- Leakage current mechanisms

Dual-switch power gating re-visited

A 32-bit carry select adder with sub-block active mode power gating

A hybrid CMOS-memristor based low power reconfigurable dynamic 4-bit multiplier

Zero-sleep-leakage Flip Flop

Summary
MOTIVATION

- The power budget limited in portable devices
- Need to maximize the battery life time
- Standby power reduction is important in implementing low power systems

Static power becomes more important with device scaling

LEAKAGE CURRENT MECHANISM IN SUB-MICRON CMOS

- $I_1$: Reverse-bias pn junction BTBT leakage
- $I_2$: Subthreshold leakage
- $I_3$: Oxide tunneling current
- $I_4$: Gate current due to hot-carrier injection
- $I_5$: GIDL
- $I_6$: Channel punchthrough current.

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Summary
HISTORY OF POWER GATING TECHNIQUES

- MTCMOS (1995)
- SCCMOS (1998)
- BGMOS (2000)
- Active PG (2004)
- Charge recycling PG (2008)
- ZSCCMOS (2003)
- Multi-sleep modes (2006)

Improvement of basic power gating (2013)
MULTI-THRESHOLD CMOS (1/2)

(a) Single footer power gating

Demerit:
- Larger area overhead
- Longer delay time
- Larger ground bounce noise
- Longer wake-up time
- Larger switching energy

(b) Single header power gating

Merit:
- Lower standby leakage current
- Compatible with CMOS process
- Compatible with the conventional EDA tools

$\mu_N > \mu_P$

Rightarrow Single footer power gating is preferable

S. Mutoh et al., “1-V power supply high-speed digital circuit technology with multithreshold voltage CMOS,” JSSC, 1995
MTCMOS (2/2)  
**Single Footer Power Gating**

- Voltage swing: $\Delta V_0 = V_{DD} = $ Full voltage swing
- Very large switching power
- Small footer area
Demerit:

- Transmission gate area overhead
- Longer wake-up time
- Larger switching energy at short sleep time
- Extra control signal needed

Merit:

- Switching power saved
- Single PG switch is used
- Small PG switch area

**Charge Recycling Power Gating (2/2)**

- $V_{SSV}$ and $V_{DDV}$ lines share charge at the sleep-in and wake-up moments by TGP and TGN
- During switching time: $\Delta V_1 = \text{Half } V_{DD}$ swing
- Switching energy is recycled up to 50% compared to the conventional PG

Traditional understanding
- Both footer and header are used for PG
- Large header and footer area overhead
- Voltage drop on these switches
- Rarely used due to slow speed during active time

Re-visited:
- Slower delay time but more power efficiency in switching and leakage power consumption than single footer and header PG

S. Mutoh et al., “1-V power supply high-speed digital circuit technology with multithreshold voltage CMOS,” JSSC, 1995
Dual Power Gating Revisited

- Voltage swing: $\Delta V_2 = \text{half } V_{DD} = \text{Half voltage swing}$
- Smaller switching power than SFPG
- DIBL effect $\Rightarrow$ smaller leakage current than SFPG and CRPG
### COMPARISON: SFPG, CRPG AND DSPG

<table>
<thead>
<tr>
<th></th>
<th>SFPG(Fig. a)</th>
<th>CRPG(Fig. b)</th>
<th>DSPG(Fig. c)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing constraint</td>
<td>Same</td>
<td>Same</td>
<td>Same</td>
</tr>
<tr>
<td>Voltage swing</td>
<td>Full $V_{DD}$</td>
<td>Half $V_{DD}$</td>
<td>Half $V_{DD}$</td>
</tr>
<tr>
<td>Switching power</td>
<td>Large</td>
<td>Small</td>
<td>Small</td>
</tr>
<tr>
<td>Power gating switch area</td>
<td>Small</td>
<td>Small</td>
<td>Large</td>
</tr>
<tr>
<td>Standby leakage power</td>
<td>Large</td>
<td>Large</td>
<td>Small</td>
</tr>
</tbody>
</table>

VOLTAGE SWING COMPARISON

<table>
<thead>
<tr>
<th></th>
<th>SFPG</th>
<th>CRPG</th>
<th>DSPG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short sleep time</td>
<td>Small swing</td>
<td>Half swing</td>
<td>Small swing</td>
</tr>
<tr>
<td>Long sleep time</td>
<td>Full swing</td>
<td>Half swing</td>
<td>Half swing</td>
</tr>
</tbody>
</table>
POWER CONSUMPTION ANALYSIS

- $t_{\text{sleep}} = 0.02\mu s$ (a): SFPG and DSPG consume smaller switching power than CRPG due to smaller swing.
- $t_{\text{sleep}} = 10\mu s$ (b): CRPG and DSPG’s switching power are half SFPG’s one due to half $V_{DD}$ switching.
- Leakage power in DSPG is the smallest.

(a) $t_{\text{sleep}} = 0.02\mu s, T=75^\circ C, V_{DD}=1.1V, 45$-nm Tech.

(b) $t_{\text{sleep}} = 10\mu s, T=75^\circ C, V_{DD}=1.1V, 45$-nm Tech.
Critical Path Delay and Wake-up Time

- Line A: 20% critical delay overhead compared to no-PG
- Line B: 10% critical delay overhead compared to no-PG
  - Effective width: $\text{EW}_{\text{PG}} = W_{\text{PG},N} + 0.5W_{\text{PG},P}$
- The fastest wake-up time among 3 PG schemes

The same constraint timing for a fair comparison

Wake-up time at delay constraint of 10% delay overhead (line B)
COMPARISON OF SLEEP ENERGY (1/2)

- The 32-bit Carry-Lookahead-Adder circuit simulated
- SFPG ~DSPG <<CRPG for short sleep time
- SFPG>>CRPR>>DSPG for long sleep time

The 20% delay overhead constraint timing for line A

The 10% delay overhead constraint timing for line B
### COMPARISON OF SLEEP ENERGY [PJ] (1/2)

<table>
<thead>
<tr>
<th>Circuits</th>
<th>$t_{\text{sleep}}$</th>
<th>$t_d$ (20% delay overhead)</th>
<th>$t_d$ (10% delay overhead)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>SFPG</td>
<td>CRPG</td>
</tr>
<tr>
<td>C432</td>
<td>0.1µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.12 (1.04)</td>
<td>2.43 (1.18)</td>
<td>2.053 (1)</td>
</tr>
<tr>
<td></td>
<td>10µs</td>
<td>6.118 (2.98)</td>
<td>4.282 (2.09)</td>
</tr>
<tr>
<td>C499</td>
<td>0.1µs</td>
<td>4.93 (1)</td>
<td>5.71 (1.16)</td>
</tr>
<tr>
<td></td>
<td>10µs</td>
<td>13.34 (2.71)</td>
<td>9.58 (1.94)</td>
</tr>
<tr>
<td>C880</td>
<td>0.1µs</td>
<td>4.57 (1.02)</td>
<td>5.21 (1.16)</td>
</tr>
<tr>
<td></td>
<td>10µs</td>
<td>13.45 (3.01)</td>
<td>9.347 (2.09)</td>
</tr>
</tbody>
</table>
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Summary
ACTIVE-MODE POWER GATING (AMPG)

- **Active leakage current**
  - Leakage current when a circuit is in active
  - Much larger (~X10 for 100 MHz) than standby leakage, 30-40% of active power in 65-nm Tech.

- **AMPG**
  - $\text{EN}_2 = "0"$: merging CLG and PG: reducing both dynamic and active power
  - $\text{EN}_2 = "1"$: the normal operation with GCLK clock

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THE CONVENTIONAL AMPG IN CSA

(a)

(b)
What is sub-block in CSA?

- One stage consists of 2 RCAs but only one is active.
- Active sub-blocks are input-vector dependent.
- Active sub-blocks are selected/unselected by carry-out signal generated in previous stage.
Unselected sub-blocks should be turned-off

- $t_{/CKE}$ is the replica delay time of critical path
- All local power switches are turned on and RCAs calculate the carry and sum during $t_{/CKE}$
- Unselected sub-blocks (RCA) are powered off during $t_{PG}$
TIMING DIAGRAM

- Replica signal, REP, delayed from LCLK by \( \Delta \) activates all adders.
- When /CKE becomes low, all blocks are turned on and carry and sum are calculated.
- After replica delay time, rising of /CKE controls PG signal for PG\(_0\), PG\(_1\).
COMPARISON OF CRITICAL PATH DELAY

- $\alpha = \frac{W_{MN0}}{W_{total}}$
- Varying $\alpha$ creates optimum critical path delay point depending on width of power switches
  - 1% delay overhead at $\alpha = 0.9$, 32-nm PTM
  - 3% delay overhead at $\alpha = 0.7$, 22-nm PTM
- 5% area overhead for SAMSUNG 0.13-µm rules

H. M. Vo et al., “Carry select adder with sub-block power gating for reducing active mode leakage,” IEICE ELEX, 2011.
COMPARISON OF TOTAL ENERGY DISSIPATION

- 21% energy saving for the proposed sub-block AMPG at 10ns cycle time for 22-nm PTM
- Crossover time is as short as 2ns and 5ns for 22-nm and 32-nm PTM, respectively
## COMPARISON OF SPEED AT GIVEN POWER BUDGET

<table>
<thead>
<tr>
<th>Power Budget</th>
<th>The conventional AMPG</th>
<th>The new sub-block AMPG</th>
</tr>
</thead>
<tbody>
<tr>
<td>100µW (32-nm PTM)</td>
<td>30ns</td>
<td>16ns</td>
</tr>
<tr>
<td>280µW (22-nm PTM)</td>
<td>50ns</td>
<td>6ns</td>
</tr>
</tbody>
</table>

![Graph showing the comparison of speed at given power budget](image)
Outline

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  - Leakage current mechanisms
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- Summary
WHAT ARE WE DOING NOW? MEMRISTOR

- A promising candidate for digital applications
  - Better power-delay metric
  - Higher device density
- Compatible with CMOS process
  - Integrating this process with a logic process on a single wafer
- Two states are switched
  - HRS represents logic “0”
  - LRS represents logic “1”

RECENT EXISTING DIGITAL MULTIPLIERS

- CMOS based array multiplier
  - Array of Full Adders and Half Adders
  - Well-known in digital applications
- ROM-based multiplier
  - Reconfigurability
  - Power, performance and area overhead are secondary
- A hybrid CMOS-memristor based static multiplier
  - Boolean equations are minimized in form of sum-of-product
  - Using OR plane for summation operation and AND plane for product operation, similarly to Programmable Logic Array
  - Memristor switches between two values HRS (stored “0”) and LRS (stored “1”)
  - Very huge static and dynamic current
  - The intermediate level voltage nodes existing
THE PROPOSED 4-BIT MULTIPLIER

○ Indicates HRS
● Indicates LRS
STRUCTURE ANALYSIS (2/2)

THE DYNAMIC
Using pre-charge and evaluation phase

CLKDB is a delayed version of CLK
COMPARISON IN PDP AND POWER

- Smaller than PDP of the static and CMOS based multiplier up to 63%, 48%, respectively
- The power consumption of CMOS based multiplier depends on the number of transitions
### Static Current Comparison

<table>
<thead>
<tr>
<th>Types of multiplier</th>
<th>Static current when clock is gated low: All=0s [μA]</th>
<th>Static current when clock is gated low: All=1s [μA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>The dynamic</td>
<td>0.0125</td>
<td>0.0123</td>
</tr>
<tr>
<td>The static</td>
<td>333</td>
<td>308.8</td>
</tr>
<tr>
<td>The CMOS based</td>
<td>0.038</td>
<td>0.074</td>
</tr>
</tbody>
</table>

- Almost-zero static power compared to the static multiplier
- 17% and 33% static current of the CMOS-based multiplier when all=1s and all=0s, respectively
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THE CONVENTIONAL SEQUENTIAL LOGIC

Sequential logic:
(a) Without leakage reduction scheme
(b) With power gating and high-VTH retention latches
(c) With zero-sleep-leakage FlipFlop using memristor retention latch.
ZERO-SLEEP-LEAKAGE FLIP FLOP

(a) Type 1

(b) Type 2
TIMING DIAGRAM

(a) Type 1

(b) Type 2
RESULTS

(a) At 25°C

(b) At 125°C
SUMMARY

- Dual power gating re-visited in comparison with SFPG and CRPG
  - Faster wake-up time
  - Smaller sleep energy loss

- A 32-bit CSA sub-block AMPG
  - 21% less power than the conventional AMPG
  - Running faster by 47% at a given power budget

- A dynamic multiplier based on hybrid CMOS-memristor is proposed
  - Smaller dynamic power consumption
  - Smaller PDP
  - Almost zero static current compared to the static multiplier
  - Static current is only 17%-35% static current of the CMOS-based array multiplier

- Zero-sleep-leakage Flip-Flop
  - FF Type2 saves up to 87% power consumption compared to Type1
  - The crossovertime of Type 2 is shortened by 97% than FF-Type1
1. **Huan Minh Vo**, Kyeong-Sik Min, “A hybrid CMOS-memristor based low power reconfigurable dynamic 4-bit multiplier”, in preparation
Thank you!